Q.P. Code: 16EC431 **R16**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

B.Tech IV Year I Semester Regular Examinations Nov/Dec 2019

VLSI Design

(Electronics & Communication Engineering)

Time: 3 hours Max. Marks: 60

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1	**a**	Derive the relationship between I_{ds} & V_{ds} in non-saturated and saturated region.	**7M**
	b	Discuss the generations of Integration Circuits.	**5M**
		OR	
2	**a**	Explain the operation of Bi-CMOS inverter and draw the different alternative structures.	**7M**
	b	Compare CMOS with Bipolar transistors in different aspects.	**5M**

UNIT-II

3	**a**	Explain the different steps involved VLSI Design flow.	**6M**
	b	Realize the layout of AND-OR-INVERTER in NMOS design Styles.	**6M**
		OR	
4	**a**	Write about Implant, demarcation line in stick diagrams with neat sketches.	**6M**
	b	Explain 2µm -based design rules with neat sketches.	**6M**

UNIT-III

5	**a**	Write short notes on (i). NORA logic. (ii). complex logic gates	**6M**
	b	Write about Power delay estimation in VLSI circuits.	**6M**
		OR	
6		What is the necessity of floor planning concept in VLSI circuits? And discuss with suitable example.	**12M**

UNIT-IV

7	**a**	Explain the working of Zero/one detector implemented with adder circuit.	**8M**
	b	Draw and Explain the circuit diagram of four bit Carry ripple adder.	**4M**
		OR	
8		Write about the following sub circuits a. Parity generators. b. Comparators.	**6M** **6M**

UNIT-V

9	**a**	Design the logic diagram of PLA for the following. Y1=A'B'C'+ABC+A'B+ABC' Y2=ABC+A'B'C+AC.	**7M**
	b	Discuss in detail about standard cell design with suitable diagrams.	**5M**
		OR	
10	**a**	What is testing? And explain any three test principles.	**6M**
	b	Compare the PROM, PAL, and PLA.	**6M**

*** END ***